



PhD EDITS 2023



5th IEEE PhD Colloquium on Emerging Domain Innovation & Technology for Society 17 & 18 November 2023, Bengaluru, India

Your Research process made EASY

Exchange your ideas and initiate dialogues with enthusiastic Scholars and mentors.

Advance your research journey.

Strengthen & shape your work from different perspectives as you progress.

Yield new insights on related problem.

IMPORTANT DATES

Paper Submission

24 September 2023
(Hard Deadline)

Acceptance Notification

06 October 2023

Camera Ready

16 October 2023

Last Date for Registration

STEERING COMMITTEE

- **Navin Kumar**,
Amrita School of Engineering, B'lore
- **Dilip Krishnaswamy**,
Founder, QWalks, New Jersey, USA
- **Sudarshan T S B**,
PES University, B'lore
- **Shikha Tripathi**,
PES University, B'lore

COLLOQUIUM MENTORS

- **Aloknath De**,
Chair, IEEE B'lore Section
- **Ganesan Thiagarajan**,
Morse Micro, New South Wales, Australia
- **Anindya Saha**
Chair, IEEE ComSoc B'lore Chapter

PhD EDITS- 2023 aims to bring together highly motivated community of PhD scholars to exchange their idea/ongoing work. The platform is very unique in the sense that it provides scholars an opportunity to directly interact one-to-one with industry expert and discuss their problem, process, direction of research. Experts from industry have agreed to be the part of the event and they will be available to discuss in the forum. At the same time; their idea, concept, process can be submitted as extended abstract which will be submitted (on acceptance and presentation in the colloquium) for publication in to IEEE Xplore for possible inclusion. Although, we currently have tracks in the domain of Electronics (including power electronics, power grid/smart grid), Communication and Computer Science and Engineering; but it would be possible to extend in any area of IEEE society interest. The colloquium is IEEE ComSoc Bangalore supported and technically sponsored by IEEE.



For further details visit: www.phdedits.in

[Click here](#)

CALL FOR EXTENDED ABSTRACT

PhD scholars at any stage of their work (not submitted their thesis) are invited to submit their ongoing work/idea/concept to this colloquium. As specified, few major domain/tracks are mentioned but we can extend to any IEEE society of interest. While, accepted and presented extended abstracts will be submitted for possible inclusion into IEEE Xplore.

TECHNICAL DOMAIN/ TRACK		VENUE
The Sub-domains include but not limited to the following topics.		AMRITA UNIVERSITY Kasavanahalli, Carmelaram P.O. Bengaluru - 560 035 Karnataka, India
Communication TCC: Lalitha H, BIT <ul style="list-style-type: none"> • Analog & Digital Communication • Wireless Communication(5G) • MIMO Systems & Cognitive Radio • mmWave Communication • Optical Communication • Antenna Theory • VLC & Quantum Communication • Satellite Communication • Coding & Information Theory 	Signal Processing TCC: Richa Tengshe, CMRIT <ul style="list-style-type: none"> • Algorithms and Architecture • Image, Audio & Video Processing • Multimedia Applications • Biomedical Applications • NLP & Applications • Communication Applications. • Pattern Analysis • Sparse Signal Processing • Graphical Signal Processing • Multivariate Signal Processing 	
Data Science, AI & Networking TCC: Sarda Sharma, ASE <ul style="list-style-type: none"> • 5G/Next Generation Networks • Heterogeneous Networks • Body Area Networks • SDN/NFV, Network Slicing • Security and Privacy • Edge & Cloud Computing • Augmented & Virtual Reality • Optical Networks and Systems • Sensor and Ad hoc Networks • Cyber-Physical Systems / IoT • Biological Networks • Computer Vision • Pattern Recognition • Machine Learning, Deep Learning • Big Data • AI/ML applications in Networks, Communication, Signal Processing & IoT 	VLSI & Embedded Systems TCC: Rajesh Chandrashekar, PESU <ul style="list-style-type: none"> • Application specific processors and devices. • Real Time Systems. • Networked Embedded Systems • Testing Techniques • AI & ML Applications • Embedded System Architecture • VLSI Circuits & design • Testing & Reliability • Post CMOS VLSI • RF Circuit Design/Analog & Mixed Mode VLSI • VLSI Applications (Communications, Video, Security, Sensor Networks, etc.) 	
		General Co-Chairs <ul style="list-style-type: none"> • Mahesh Kumar Jha, CMRIT, B'lore • Richa Tengshe, CMRIT, B'lore Technical Program Co-Chairs <ul style="list-style-type: none"> • Shachi P, BMSCE, B'lore • Lalitha H, BIT, B'lore • Preet Kanwal, PESU, B'lore • Sarda Sharma, ASE, B'lore Publication Co-Chairs <ul style="list-style-type: none"> • Monika Singh, CMRIT, B'lore • Geetika Srivastava, ASE, B'lore • Deborsi Basu, IIT KGP Sponsors & Exhibits Co-Chair <ul style="list-style-type: none"> • Rajesh Chandrashekar, PESU, B'lore • Prajeesha, PESU, B'lore • Amar Choudhary, ASE, B'lore Website Co-Chairs <ul style="list-style-type: none"> • Aritri Debnath, CMRIT, B'lore • Ramya V, ASE, B'lore Finance Co-Chairs <ul style="list-style-type: none"> • Bighnaraj Panigrahi, Nokia, B'lore • Mahesh Kumar Jha, CMRIT, B'lore • Sagar Basavaraju, ASE, B'lore Publicity Co-Chairs <ul style="list-style-type: none"> • Revathi, PESU, B'lore • Gayathri T, PESU, B'lore • Raveesh Hegde, CMRIT, B'lore • Sricheta Parui, IIT KGP • Sreebha Bhaskaran, ASE, B'lore Local Arrangement <ul style="list-style-type: none"> • Arya, R, ASE, B'lore • Vignesh V, ASE, B'lore

CONTACT US

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